IN THE CLAIMS

Please add claims 26 and 27.

Please amend claim 15 as follows:

1-9. (Cancelled)

10. (Previously Presented) An electronic component comprising:

a stack of semiconductor chips having a first semiconductor chip and a stacked second semiconductor chip, the semiconductor chips having an active first face with contact pads to integrated circuits and a second face;

a flat conductor structure having a chip island, flat conductors surrounding the chip island, and contact pillars arranged on the flat conductors and aligned orthogonally with respect to the flat conductors;

wherein the second semiconductor chip is arranged with its second face on the chip island and wherein its contact pads are electrically connected via bonding wire connections to the flat conductors;

wherein the first semiconductor chip is surrounded by the contact pillars and is arranged underneath the chip island such that pillar contact pads of the contact pillars, first face areas of a plastic encapsulation compound that embeds the semiconductor chips, the contact pillars and the flat conductor structure, and the active first face of the first semiconductor chip, form an overall first face,

wherein a wiring layer is arranged on the overall first face and electrically connects the semiconductor chips to one another via wiring lines, and

wherein the flat conductors extend to edge faces of the plastic encapsulation compound.

11. (Previously Presented) The electronic component of claim 10, wherein the wiring layer comprises a wiring level arranged on the overall first face and comprises outer contact pads that

are electrically connected via the wiring lines to the pillar contact pads of the contact pillars, and/or to the contact pads on the first semiconductor chip.

12. (Previously Presented) The electronic component of claim 10, wherein solder balls are arranged on the outer contact pads.

13. (Previously Presented) The electronic component of claim 10 configured within a panel comprising a leadframe with additional electronic components arranged in rows and columns.

14. (Previously Presented) The electronic component of claim 13, wherein the shape of the panel corresponds in its extent and extent markings to a standard semiconductor wafer.

15. (Currently Amended) A method for production of a panel for a plurality of electronic components comprising:

producing a leadframe with component positions arranged in rows and columns, whereby [[a]] each component position comprises a chip island and flat conductors which surround the chip island, as well as contact pillars, which are arranged on the flat conductors and are aligned orthogonally with respect to the flat conductors, and wherein the flat conductors extend between neighboring chip islands;

applying a plurality stacked semiconductor chips to the chip islands of the component positions;

producing bonding wire connections between the flat conductors and contact pads on active first faces of the stacked semiconductor chips;

applying first semiconductor chips with their active first faces to a carrier with adhesive bonding on one side, with the first semiconductor chips being arranged in rows and columns which correspond to the rows and columns of the component positions;

applying the leadframe with a plurality of stacked semiconductor chips to the carrier in such a way that the contact pillars of the leadframe are adhesively bonded by their first faces to

the carrier and the first semiconductor chips are arranged on the carrier underneath the chip islands of the leadframe and are surrounded by contact pillars;

embedding the leadframe with stacked semiconductor chips and bonding wire connections in a plastic compound to form a composite body on the carrier;

removing the carrier exposing an overall first face composed of active first faces of the first semiconductor chips, pillar contact pads of the contact pillars, and an first face of the plastic compound;

applying a wiring layer to the overall first face, forming wiring lines and outer contact pads; and

wherein the wiring lines connect the outer contact pads to the contact pads of the first semiconductor chip, and/or to the pillar contact pads of the contact pillars.

16. (Previously Presented) The method of claim 15 further comprising applying solder balls to the outer contact pads to provide outer contacts.

17. (Previously Presented) The method of claim 15 further comprising separating the panel into individual electronic components.

18. (Previously Presented) The method of claim 17 further comprising applying outer contact pads of an electronic component.

19. (Previously Presented) An electronic component comprising:

a first semiconductor chip having an active first face, contact pads, and a second face;

a stacked second conductor chip having an active first face, contact pads, and a second face;

a chip island;

flat conductors surrounding the chip island;

contact pillars arranged on the flat conductors and surrounding the first semiconductor

chip;

wherein the second semiconductor chip is arranged with its second face on the chip island;

means for electrically connecting the contact pads of the second semiconductor chip to the flat connectors;

a plastic encapsulation compound configured to embed the first and second semiconductor chips, the contact pillars, the chip island, and the flat conductors, wherein the flat conductors extend to edge faces of the plastic encapsulation compound;

wherein the first semiconductor chip is arranged under the chip island such that pillar contact pads of the contact pillars, first face areas of the plastic encapsulation compound, and the active first face of the first semiconductor chip form an overall first face; and

means on the overall first face for electrically connecting the first and second semiconductor chips to each other.

20. (Previously Presented) The electronic component of claim 19, wherein the contact pads of the second semiconductor chip are electrically connected to the flat conductors via bonding wire connections.

21. (Previously Presented) The electronic component of claim 19 further comprising a wiring layer arranged on the overall first face and electrically connecting the first and second semiconductor chips to each other via wiring lines.

22. (Previously Presented) The electronic component of claim 21, wherein the wiring layer comprises a wiring level arranged on the overall first face and comprises outer contact pads that are electrically connected via the wiring lines to the pillar contact pads of the contact pillars and to the contact pads on the first semiconductor chip.

23. (Previously Presented) The electronic component of claim 19, wherein solder balls are

arranged on the out contact pads.

24. (Previously Presented) The electronic component of claim 19 configured with a panel comprising a leadframe with additional electronic components arranged in rows and columns.

25. (Previously Presented) The electronic component of claim 24, wherein the shaped of the panel corresponds in its extent and extent markings to a standard semiconductor wafer.

26. (New) The electronic component of claim 11, wherein the wiring layer further comprises an insulation layer situated between the overall first face and the wiring level, the insulation layer having through contacts that electrically connect the outer contact pads to the pillar contact pads of the contact pillars and/or to the contact pads on the first semiconductor chip.

27. (New) The electronic component of claim 26, wherein the wiring layer further comprises a solder resist layer is arranged on the wiring level, the solder resist layer having openings that leave the outer contact pads 20 free.